



CAEN Educational Handbook

Nuclear and Particle Physics Experiments



<https://edu.caen.it>

MULTICHANNEL READOUT USING THE ROUND ROBIN ARBITER

SG6319F



SP5650 - OPEN FPGA KIT

Difficulty



Execution Time



Purpose of the experiment

This experiment introduces the concept of multichannel data acquisition and shows how multiple input channels can be managed. Students learn how several channels can share the same processing and readout resources in a controlled and efficient way.

Fundamentals

In multichannel acquisition systems, several input channels may generate events simultaneously. Since the processing and readout resources are often shared, a method is required to decide which channel is processed at a given time. A common solution is the

Round Robin arbiter, which cyclically scans all channels and assigns processing time to each one in sequence. If a channel has data ready, it is served; otherwise, the system moves to the next channel. This method ensures fair access to shared resources and prevents any single channel from monopolizing the system. Round Robin arbitration is widely used in digital electronics and data acquisition systems to manage multiple data streams efficiently.

Requirements

Python environment.

Carrying out the experiment

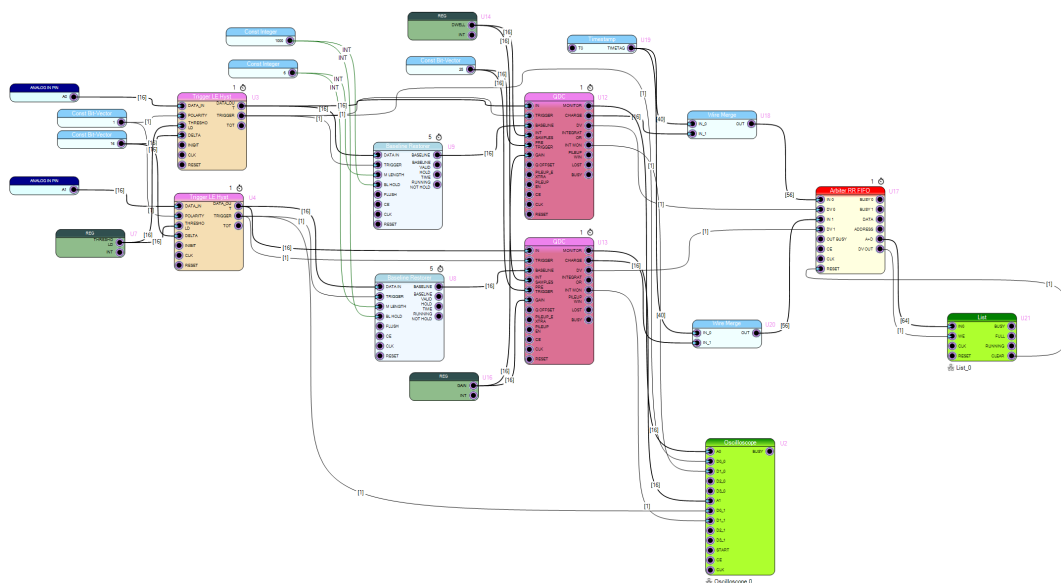
A firmware design is implemented including multiple input channels connected to a shared processing chain and readout interface. A Round Robin arbiter controls which channel is processed at each cycle. Input signals are applied to multiple channels, and the arbiter sequentially grants access to the processing and readout blocks. The acquired data are then transferred to the PC and monitored using the control software.



Experimental setup block diagram.

Results

This experiment demonstrates how the Round Robin arbitration method is used in multichannel data acquisition systems to manage shared resources efficiently and ensure fair channel access. Students can observe how the system handles multiple channels and how the arbitration logic distributes processing time among them.



Design Schematics.