# CAEN Educational Handbook

## Nuclear and Particle Physics Experiments

https://edu.caen.it

# SUB-BLOCK INSTANCES SG6321F

SP5650 - OPEN FPGA KIT

Difficulty Execution Time

## Purpose of the experiment

This experiment introduces the use of sub-block instances in FPGA design. Students learn how a functional block can be instantiated multiple times within a project, allowing efficient implementation of repetitive structures such as multichannel processing chains.

## Fundamentals

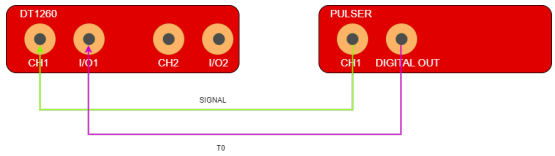
In FPGA design, complex systems are often built using hierarchical and modular design techniques. Instead of creating large monolithic designs, smaller functional blocks can be developed and reused multiple times. A sub-block instance is a copy of a functional block that operates independently but shares the same internal structure. This approach is useful when the same processing operation must be applied to multiple signals, such as in multichannel readout systems. Using sub-block instances improves design scalability, simplifies debugging, and reduces development time.

## Requirements

Python environment.

## Carrying out the experiment

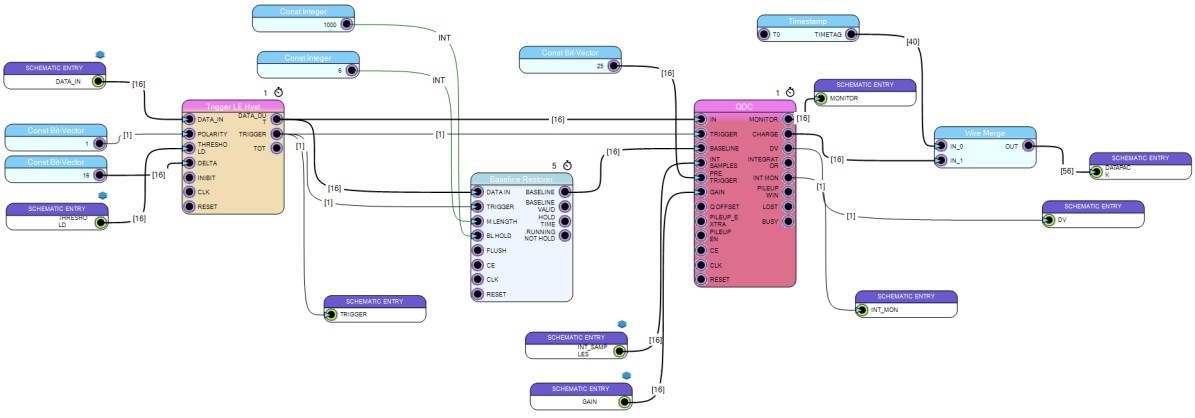
Activate your Sci-Compiler license and set up the software installation. Plug the USB dongle into your PC and launch Sci-Compiler. Create a new project for your DT1260 unit by clicking New Project. A firmware design is implemented by creating a functional processing block and then generating multiple instances of this block within the main design. Each instance processes its own input signal independently. The outputs of the different block instances are connected to shared resources such as memory buffers or readout modules. Input signals are provided to the board using a pulse generator connected to multiple inputs. The FPGA processes the signals through the different block instances, and the results are then made available to the control software.




Experimental setup block diagram.

## Results

The system successfully processes multiple input signals using replicated sub-block instances. Each instance operates independently while sharing common readout resources. This experiment demonstrates how hierarchical design and block instantiation can be used to implement scalable multichannel systems in FPGA-based data acquisition applications.



Block diagram of the sub-design.